

# NTMKE4890N

## Power MOSFET 30 V, 155 A, Single N-Channel, ICEPAK

### Features

- Low Package Inductance
- Low  $R_{DS(on)}$  to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- Optimized Gate Charge to Minimize Switching Losses
- Dual Sided Cooling Capability
- Compatible with MX Footprint and Outline
- These are Pb-Free Devices

### Applications

- CPU Power Delivery
- DC-DC Converters
- Optimized for both Synch FET

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise stated)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	$V_{DSS}$	30	V
Gate-to-Source Voltage	$V_{GS}$	$\pm 20$	V
Continuous Drain Current $R_{\theta JA}$ (Note 1)	$I_D$	$T_A = 25^\circ\text{C}$	32
		$T_A = 70^\circ\text{C}$	25.5
Power Dissipation $R_{\theta JA}$ (Note 1)	$P_D$	2.8	W
Continuous Drain Current $R_{\theta J-PCB}$ (Note 2)	$I_D$	$T_A = 25^\circ\text{C}$	155
		$T_A = 70^\circ\text{C}$	86
Power Dissipation $R_{\theta J-PCB}$ (Note 2)	$P_D$	$T_A = 25^\circ\text{C}$	65
		$T_C = 25^\circ\text{C}$	192
Continuous Drain Current $R_{\theta JC}$ (Note 1)	$I_D$	$T_C = 25^\circ\text{C}$	154
		$T_C = 25^\circ\text{C}$	100
Power Dissipation $R_{\theta JC}$ (Note 1)	$P_D$	100	W
Pulsed Drain Current	$T_A = 25^\circ\text{C}, t_p = 10 \mu\text{s}$	$I_{DM}$	244
Current Limited by Package	$T_A = 25^\circ\text{C}$	$I_{Dmax}$	50
Operating Junction and Storage Temperature	$T_J, T_{stg}$	-40 to	$^\circ\text{C}$
		150	
Source Current (Body Diode) (Note 1)	$I_S$	128	A
Drain to Source DV/DT	dV/dt	6.0	V/ns
Single Pulse Drain-to-Source Avalanche Energy ( $T_J = 25^\circ\text{C}, V_{DD} = 30 \text{ V}, V_{GS} = 10 \text{ V}, I_L = 58 \text{ A}_{pk}, L = 0.3 \text{ mH}, R_G = 25 \Omega$ )	$E_{AS}$	505	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	$T_L$	270	$^\circ\text{C}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

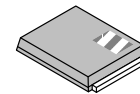
1. Surfaced mounted on FR4 board using 1 sq-in pad, 1 oz Cu.
2. Measured with a  $T_J$  of approximately  $90^\circ\text{C}$  using 1 oz Cu board.
3. Surfaced mounted on FR4 board using 1 sq-in pad, 2 oz Cu.



ON Semiconductor®

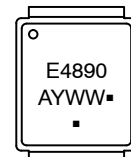
<http://onsemi.com>

$V_{(BR)DSS}$	$R_{DS(ON)} \text{ MAX}$	$I_D \text{ MAX}$
30 V	1.8 m $\Omega$ @ 10 V	155 A
	2.5 m $\Omega$ @ 4.5 V	

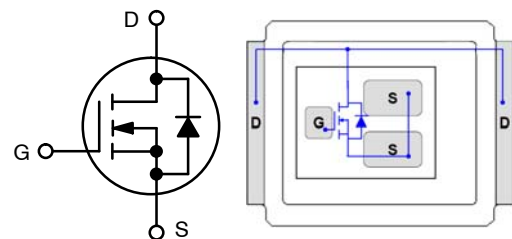


ICEPAK  
E PAD  
CASE 145AB

### MARKING DIAGRAM



E4890 = Specific Device Code  
 A = Assembly Location  
 Y = Year  
 WW = Work Week  
 ■ = Pb-Free Package  
 (Note: Microdot may be in either location)



N-CHANNEL MOSFET

### ORDERING INFORMATION

Device	Package	Shipping†
NTMKE4890NT1G	ICEPAK (Pb-Free)	1500/Tape & Reel
NTMKE4890NT3G	ICEPAK (Pb-Free)	5000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

# NTMKE4890N

## THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case (Drain) (Note 1)	$R_{\theta JC}$	1.25	°C/W
Junction-to-Ambient – Steady State (Note 1)	$R_{\theta JA}$	45	
Junction-to-Ambient – Steady State (Notes 2 and 3)	$R_{\theta JA}$	25	
Junction-to-PCB (Note 2)	$R_{\theta J-PCB}$	1.0	

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	30			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$			20		mV/°C
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{GS} = 0\text{ V}, V_{DS} = 24\text{ V}$			1.0	$\mu\text{A}$
					100	
Gate-to-Source Leakage Current	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			$\pm 100$	nA

### ON CHARACTERISTICS (Note 4)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\ \mu\text{A}$	1.4		2.4	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			5.9		mV/°C
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 30\text{ A}$		1.5	1.8	m $\Omega$
		$V_{GS} = 4.5\text{ V}, I_D = 30\text{ A}$		2.1	2.5	
Forward Transconductance	$g_{FS}$	$V_{DS} = 15\text{ V}, I_D = 25\text{ A}$		120		S

### CHARGES, CAPACITANCES AND GATE RESISTANCE

Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}, V_{DS} = 15\text{ V}$		7100		pF
Output Capacitance	$C_{oss}$			1360		
Reverse Transfer Capacitance	$C_{rss}$			690		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 15\text{ V}, I_D = 25\text{ A}$		51.7		nC
Threshold Gate Charge	$Q_{G(TH)}$			6.0		
Gate-to-Source Charge	$Q_{GS}$			18.8		
Gate-to-Drain Charge	$Q_{GD}$			18.6		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 10\text{ V}, V_{DS} = 15\text{ V}, I_D = 25\text{ A}$		104		nC

### SWITCHING CHARACTERISTICS (Note 5)

Turn-On Delay Time	$t_{d(on)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 15\text{ V}, I_D = 25\text{ A}, R_G = 2.0\ \Omega$		25		ns
Rise Time	$t_r$			23		
Turn-Off Delay Time	$t_{d(off)}$			42		
Fall Time	$t_f$			12		

### DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	$V_{SD}$	$V_{GS} = 0\text{ V}, I_S = 20\text{ A}$	$T_J = 25^\circ\text{C}$	0.78	1.0	V
			$T_J = 125^\circ\text{C}$	0.68		
Reverse Recovery Time	$t_{RR}$	$V_{GS} = 0\text{ V}, dI_S/dt = 200\text{ A}/\mu\text{s}, I_S = 20\text{ A}$		41.8		ns
Charge Time	$t_a$			19.4		
Discharge Time	$t_b$			22.4		
Reverse Recovery Charge	$Q_{RR}$			61		nC

### PACKAGE PARASITIC VALUES

Gate Resistance	$R_G$	$T_A = 25^\circ\text{C}$		0.6	1.5	$\Omega$
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4. Pulse Test: pulse width = 300  $\mu\text{s}$ , duty cycle  $\leq 2\%$ .

5. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

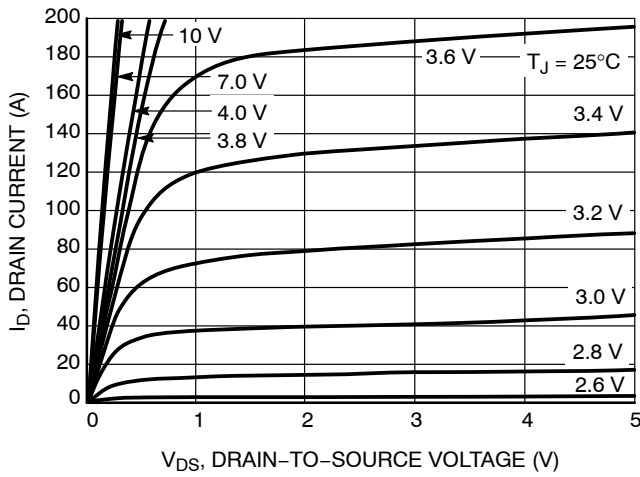


Figure 1. On-Region Characteristics

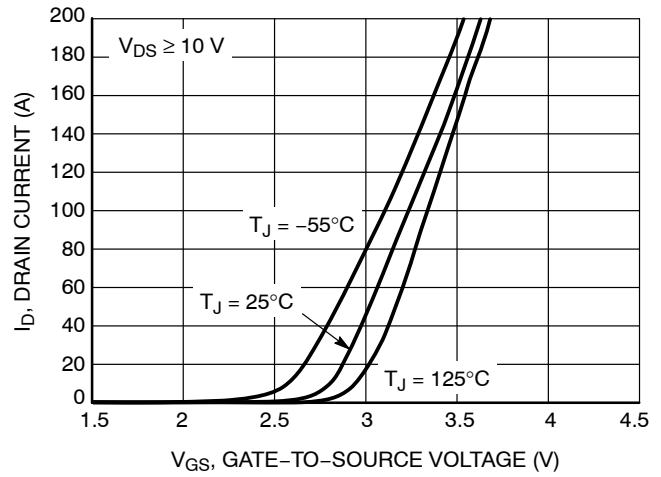


Figure 2. Transfer Characteristics

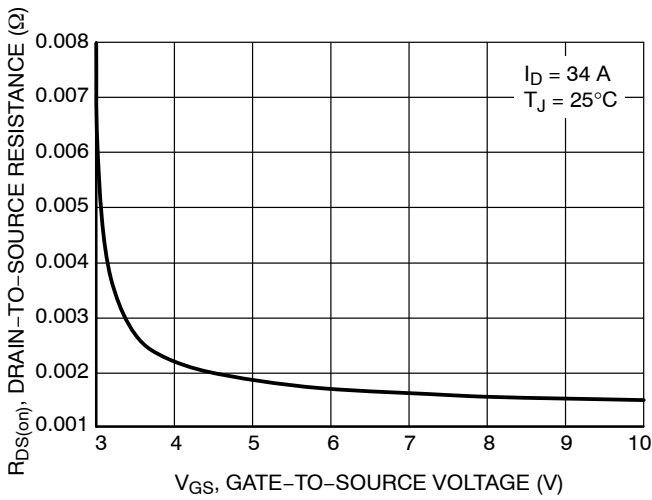


Figure 3. On-Resistance vs. Gate-to-Source Voltage

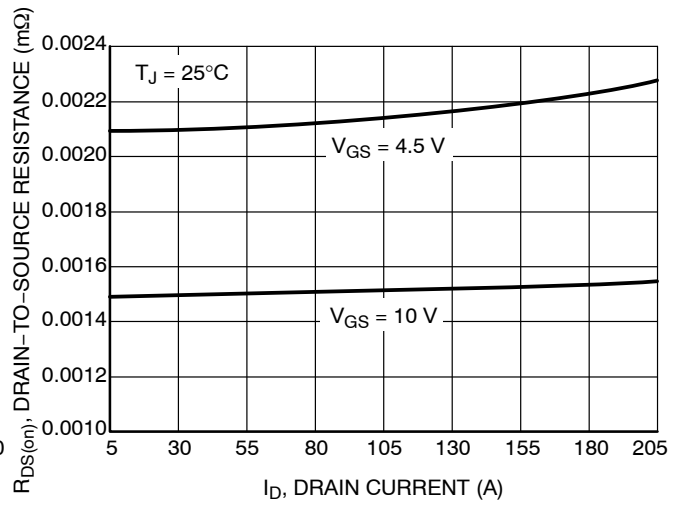


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

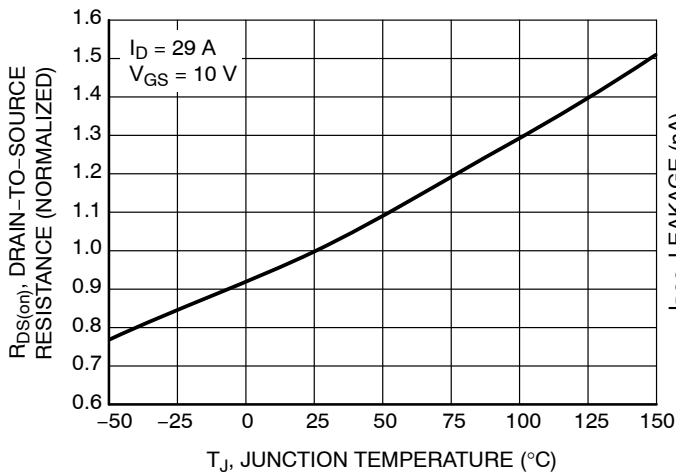


Figure 5. On-Resistance Variation with Temperature

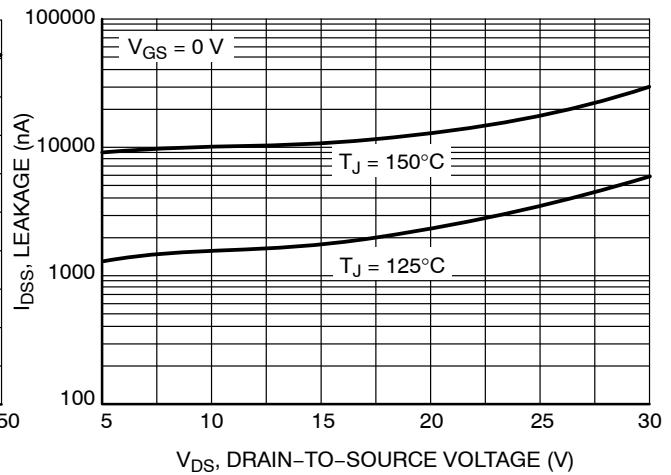
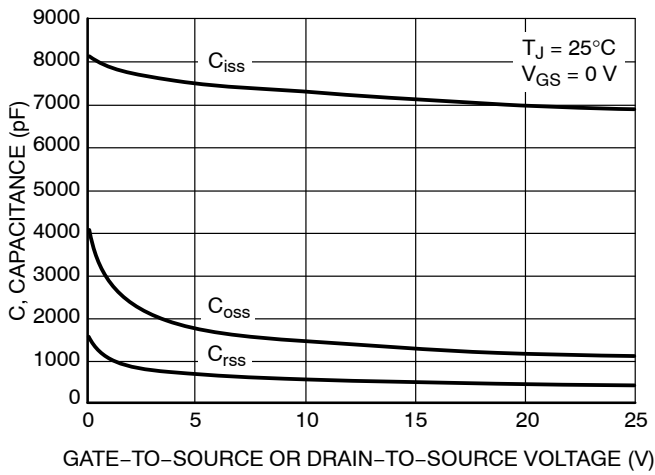


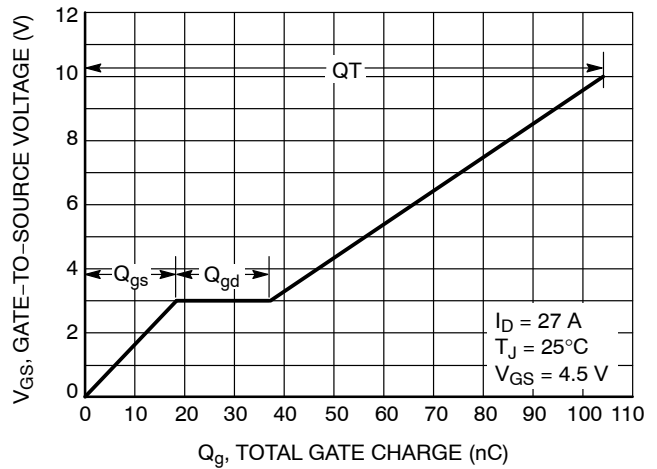
Figure 6. Drain-to-Source Leakage Current vs. Voltage

# NTMKE4890N

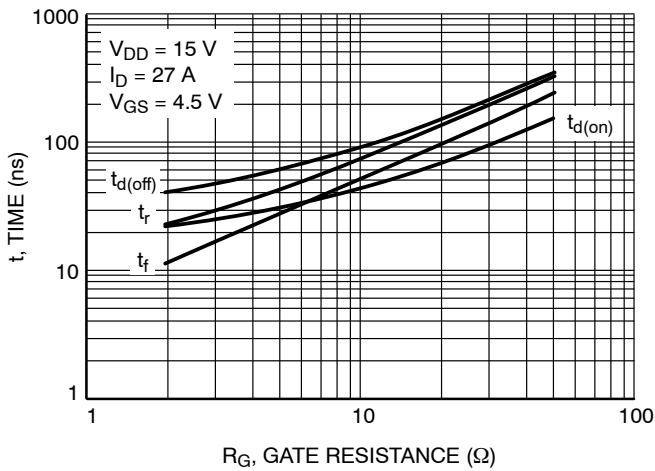
## TYPICAL CHARACTERISTICS



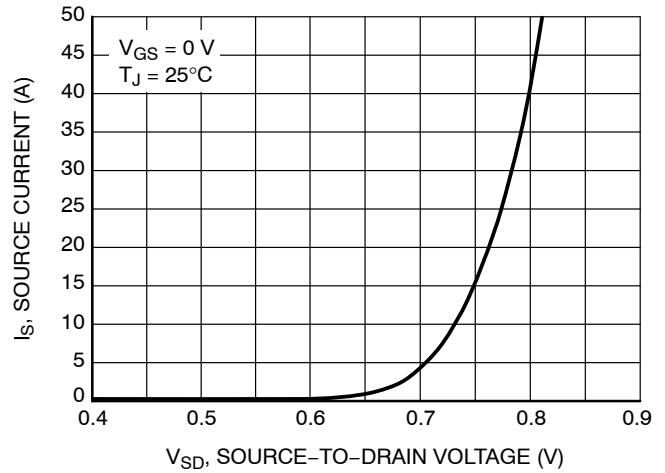
**Figure 7. Capacitance Variation**



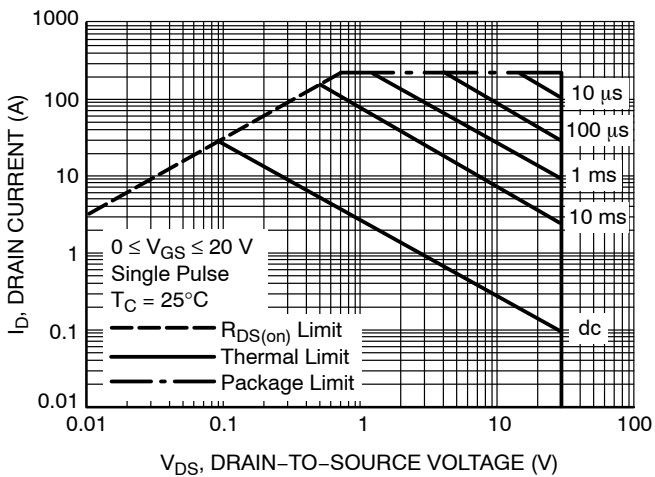
**Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge**



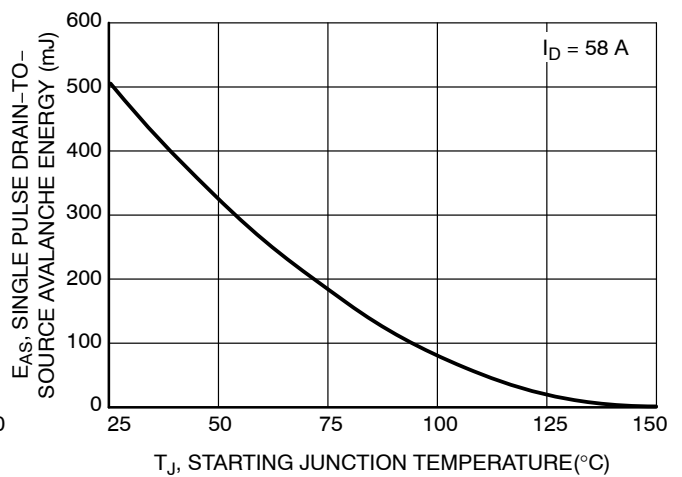
**Figure 9. Resistive Switching Time Variation vs. Gate Resistance**



**Figure 10. Diode Forward Voltage vs. Current**



**Figure 11. Maximum Rated Forward Biased Safe Operating Area**



**Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature**

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## TYPICAL CHARACTERISTICS

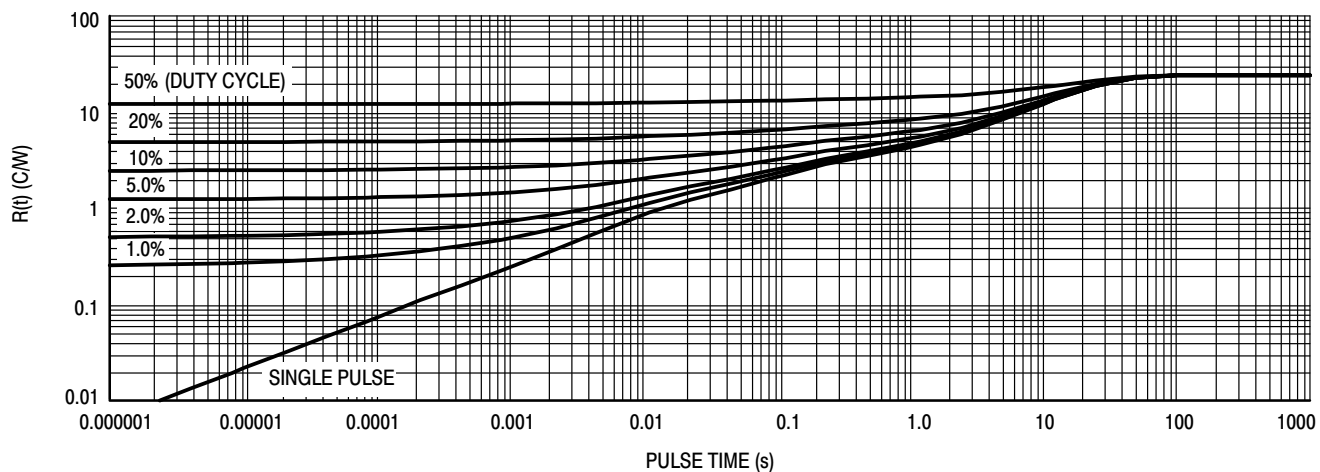
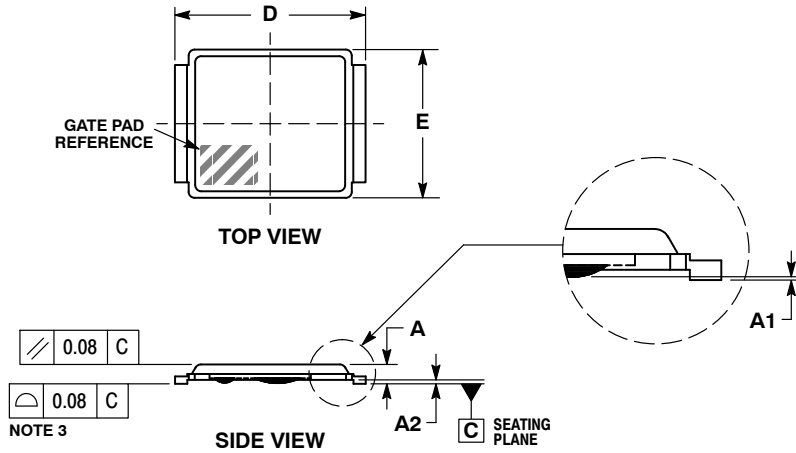


Figure 13. Thermal Impedance

# NTMKE4890N

## PACKAGE DIMENSIONS

ICEPAK 6.3x4.9 – E PAD  
CASE 145AB-01  
ISSUE 0

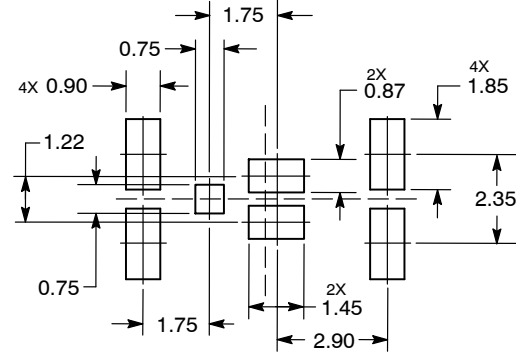
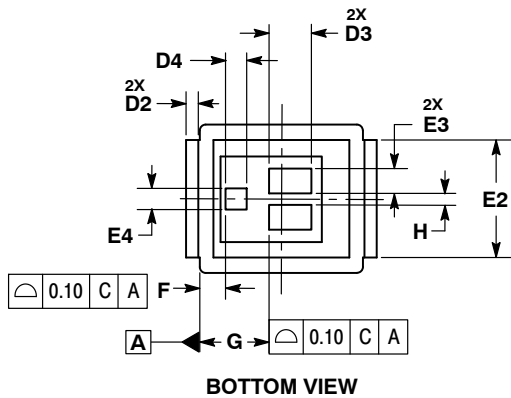


**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO THE FLANGES OF LEADFRAME ONLY.

DIM	MILLIMETERS	
	MIN	MAX
A	0.61	0.68
A1	0.02	0.08
A2	0.08	0.17
D	6.25	6.35
D2	0.35	0.45
D3	1.38	1.42
D4	0.68	0.72
E	4.80	5.05
E2	3.85	3.95
E3	0.80	0.84
E4	0.68	0.72
F	0.94 BSC	
G	2.54 BSC	
H	0.38	0.42

### SOLDERING FOOTPRINT\*



DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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